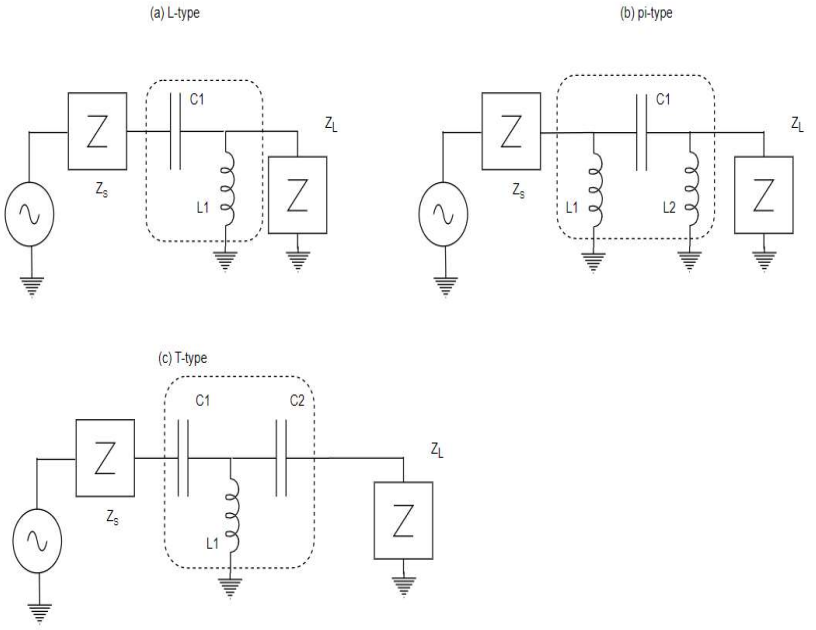
This design note discusses impedance matching networks connecting RF sources to loads. Specifically, it covers narrow-band applications. Below are three general topologies referred to as L, π and T matching circuits. The name comes from the schematic shape.

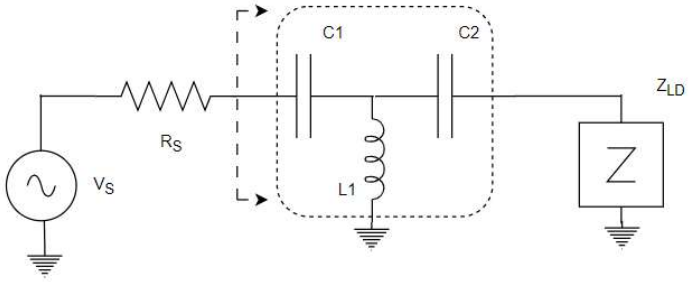
Figure 1 – Impedance matching circuits



The topologies above have a common characteristic; they block DC. The above topologies can be modified by interchanging capacitors and inductors to make the circuit pass DC. All six topologies are valid impedance matching networks.

For purposes of this article we will use the T-type shown in figure 1(c). We will also assume the source impedance is the real value R_S. The circuit we will be working with is shown in figure 2:

Figure 2 – T-type impedance matching



The objective of the T network is to “look” into the T-network from the source port and see a real impedance of Rs and ideally zero reactance at the frequency of interest f_0. The problem can be described as:

Given Rs, Z_{LD} and f_o, design C1, C2 and L1 to achieve zero reflections at the input port.

Circuit Preliminaries

The design approach used in this article is sometimes called the Q method. The impedance of C2 in series with Z_{LD} is computed and converted to an equivalent parallel impedance in terms of a desired parallel Q at frequency f0 and the value of L1 is chosen to cancel the reactance. To explain this more clearly in general terms, assume a series impedance to ground $Z_S = R_S + j\cdot X_S$. The series impedance is:

$$Zin = R_S + j\cdot X_S \quad [1]$$

For two elements Rp and j·Xp in parallel the impedance is:

$$Zin = Rp\cdot jXp / (Rp + j\cdot Xp) \quad [2]$$

$$= Rp\cdot jXp \cdot (Rp - j\cdot Xp) /(Rp^2 + (Xp)^2)$$

$$= Rp\cdot(Xp)^2/((Rp^2 + (Xp)^2) + j\cdot(Rp)^2\cdot Xp/((Rp^2 + (Xp)^2)$$

Now, we define the loaded parallel Qp = Rp/Xp and series loaded Qs = Xs/Rs, we can rewrite Zin as:

$$Zin = Rp / (1 + (Qp)^2) + j\cdot(Qp)^2\cdot Xp/(1 + (Qp)^2) \quad [3]$$

Finally, we can equate [1] and [3] to arrive at:

$$R_S = Rp / (1 + (Qp)^2) \text{ or,} \quad [4a]$$

$$Rp = Rs\cdot(1 + (Qp)^2) \quad [4b]$$

Equation [4] shows that a series resistance gets converted to a higher parallel resistance determined by the value of Qp. Conversely, converting a parallel resistance to a series circuit lowers the resistance determined by the value of Qp.

Similarly, for series reactance, Xs, gets converted to a lower parallel reactance given by [5],

$$X_S = (Qp)^2\cdot Xp / (1 + (Qp)^2) \text{ or,} \quad [5a]$$

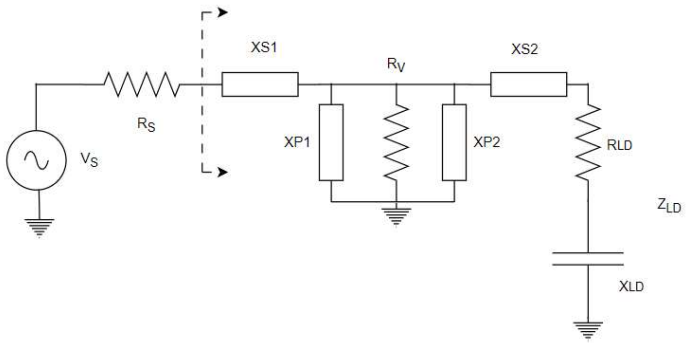
$$Xp = Xs\cdot(1 + (Qp)^2)/(Qp)^2 \quad [5b]$$

As an example, for Rs = 2.0 ohms and Xs = j80 ohms a Qp of 10 will convert these series values to the parallel values Rp= 202 ohms and Xp = 80.08 ohms. If Xs is a capacitor the parallel equivalent is a smaller capacitor value while if Xs is an inductor the parallel conversion results in a larger value inductor. Converting between parallel and series circuits using a selected Q is the method to solve the matching network design.

Back to the Design Example

For the design example the source impedance is Rs = 50 ohms, the frequency is 13.54MHz and the load impedance is a series RC with impedance Z_{LD} = 2.0 - j4.0 ohms at f0. A schematic of the circuit is below, with some additions to aide in explaining the design process.

Figure 3 – Example



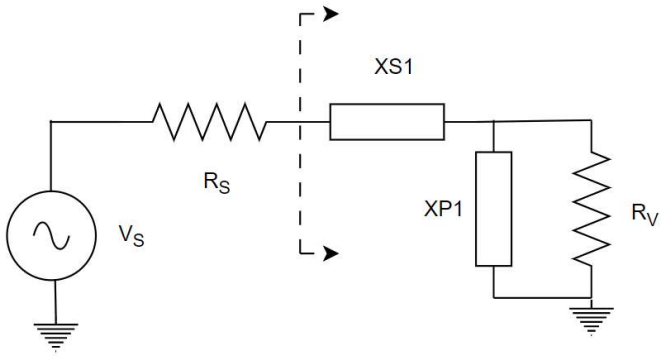
In figure 3 the T-network is drawn to show the input series capacitor XS1 and output series capacitor XS2. The parallel inductor is drawn as two segments, XP1 and XP2. This highlights the T-network can be considered to L-network. The parallel resistor, Rv, is a virtual resistor that does not exist in the real circuit. This will be explained later.

The series output circuit X_{S2} + R_{LD} + X_{LD} needs to be expressed as the equivalent real and reactive components, Zin = R_{LD} – j(X_{S2}+X_{LD}). We can then use the definition of series Q and state that (X_{S2}+X_{LD}) = 20.0. From this we can conclude X_{S2} = (20-4) = 16 ohms capacitive. Using Zin = R_{LD} – j(X_{S2}+X_{LD}) = 2.0 -j20.0, we can compute the parallel equivalent impedance using [4b] and [5b] as,

$$Zp = 101 \cdot 2 - j\ 101 \cdot 20/100 = 202 - j \cdot 20.2 \qquad [6]$$

In [6] the real portion, 202 ohms, represents the virtual impedance Rv shown in figure 3. In order to cancel out the reactive component we set X_{P2} to be the equal and opposite inductor with 20.2 ohms at f0. The circuit in figure 3 can now be replaced with this schematic.

Figure 4 – Simplified schematic for input side



In figure 4 we have so far defined Rv, (202 ohms) and we need to use the L-network (XS1,XP1) to transform the 202 ohm real resistance to Rs = 50 ohms and chose X_{P1} and X_{S1} to cancel the reactive component. We can use [4b] and compute the needed Qp as sqrt(Xp/Xs -1) = 1.743.

Now, using the definition of Qp= Rp/Xp, we compute Xp = 115.89. The last step is to calculate X_{S1} using [5a], $X_{S1}= X_{P1}\cdot(Q_P)^2/ (1 + (Q_P)^2) = 87.19$

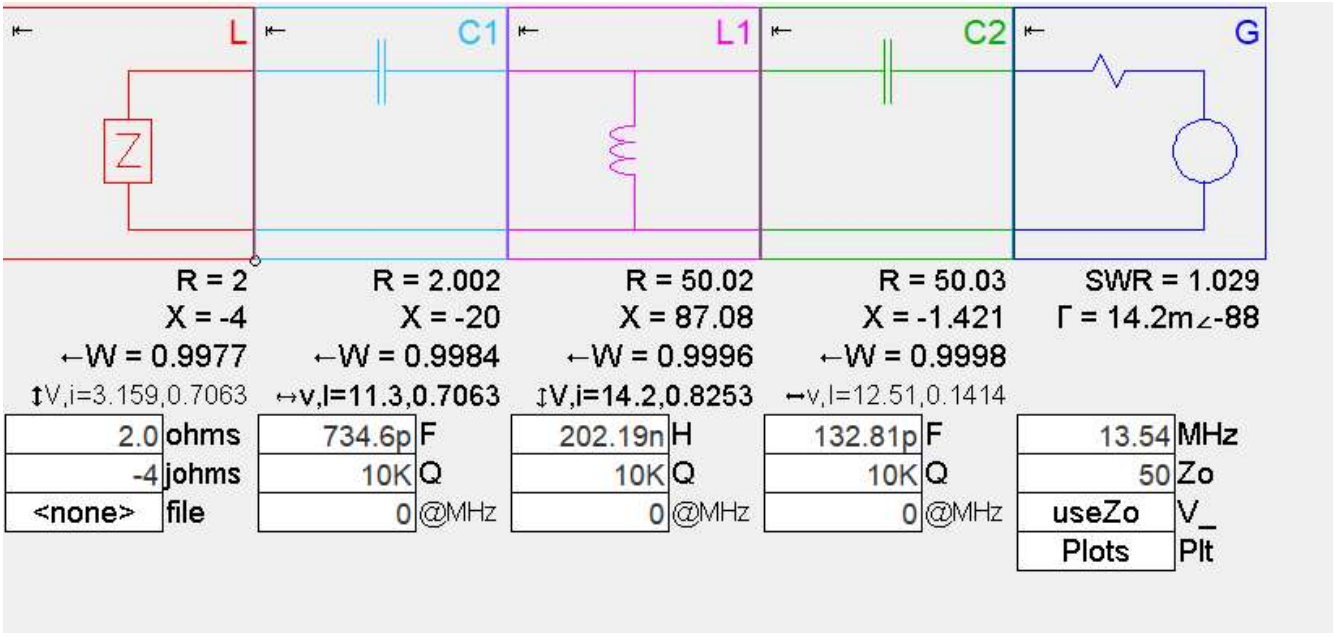
Table 1 – Component value summary

Component	Impedance @ 13.54MHz	Component Value
XS1	87.19	132.81pf
XP1	115.89	8.559uh
XS2	16.0	734.6pf
XP2	20.2	237.4nh
XP1 // XP2	17.201	202.19nh
Xld	2-j4.0	

Smith Chart

We will now use SimChart and LTspice to look at a frequency sweep of the final matching network. Consider the circuit shown in figure 5.

Figure 5 – Sim-Chart Schematic



The generator side G has an impedance Z_o = 50 ohms. The load, L, has a complex impedance Z_L= 2.0-j4.0. The network comprised of C1, C2 and L1 is a T-type impedance matching network. The narrow-band match is at frequency fo= 13.54Mhz. To compare this to the calculated values I used the calculated values and not standard component values.

The next figure shows the Smith chart scan from 5Mhz to 20Mhz. The circle in the very center is a near perfect match (50.2 ohms) at 13.54Mhz (SWR = 1.029).

Figure 6 – Smith Chart Scan

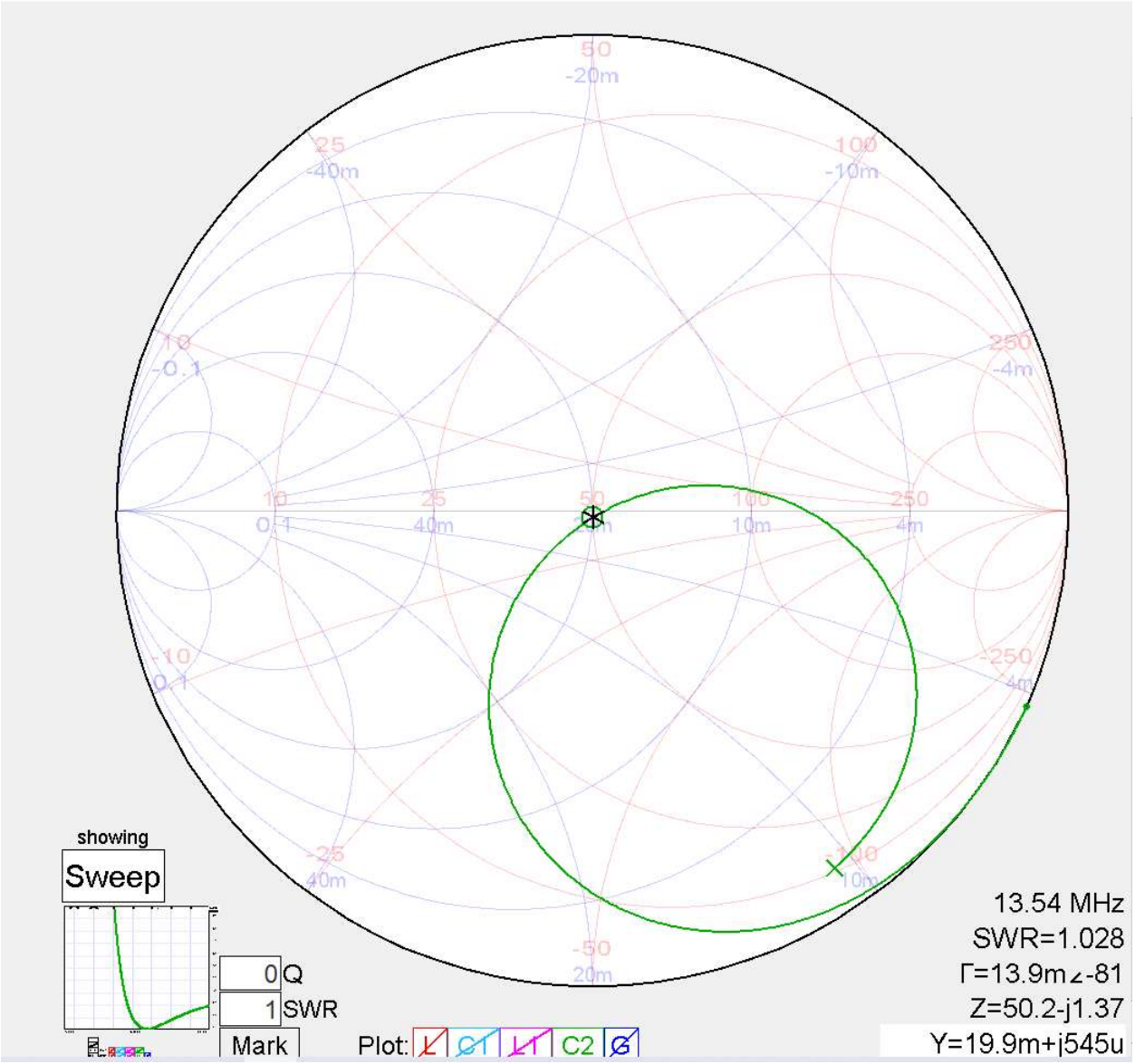


Figure 7 – LTspice sweep 1Mhz to 20Mhz showing power into load peaking at 13.54MHz

Look at Tuning

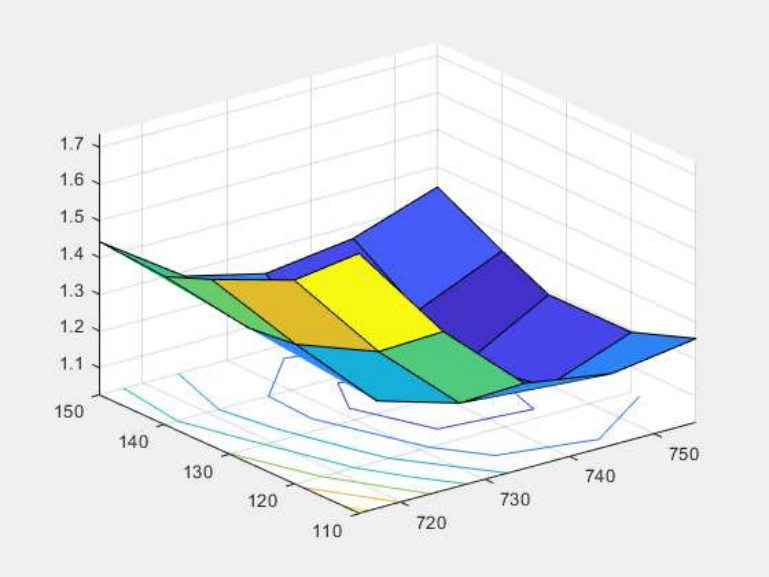
This section will look at adjusting capacitors C1 (XS1) and C2 (XS2). The Smith Chart will be used to adjust C1 and C2 over a grid and record the magnitude of VSWR. Then that surface will be viewed to see if it is convex.

Table 2 – Plot VSWR surface versus (C1,C2)

C1 / C2	110	120	132.81	140	150
715	1.737	1.462	1.261	1.223	1.256
725	1.583	1.326	1.126	1.107	1.192
734.6	1.481	1.242	1.028	1.064	1.190
745	1.430	1.227	1.114	1.151	1.251
755	1.443	1.288	1.235	1.266	1.344

The contour plot is shown in the next figure,

Figure 8 – Surface plot VSWR versus (C1,C2)



The VSWR data in Table 2 appears to be convex with a minimum at (734.6,132.81). The surface plot in figure 8 also confirms the VSWR to be a convex hull. The implications of this are the impedance

matching circuit can be tuned automatically by measuring VSWR and adjusting C1 and C2 using an algorithm for global optimization.

Conclusion

The equations for a narrow-band impedance matching circuit has been derived for the T-type network. It has been shown the matching can be tuned by adjusting two capacitors. The tuning can be achieved by monitoring the VSWR and adjusting the two capacitors using a global optimization algorithm.